IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/896,345	Confirmation No. 8325
Applicant	:	**Soumyanath, K.**	
Filed	:	**28 June 2001**	
TC/AU	:	**2816**	
Examiner	:	**Nguyen, H. L.**	
Docket No.	:	**p11206**	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Appeal Brief under 37 C.F.R. §1.192

Assistant Commissioner for Patents:

The applicant ("Applicant") respectfully submits this Brief in triplicate in support of his appeal from a decision by the Examiner to twice reject the claims in the above-identified case.

An oral hearing is not desired.

1.   Real Party of Interest

Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052, is the assignee of the present invention and the real party of interest.

2.   Related Appeals and Interferences

To the best of Applicants' knowledge, there are no appeals or interferences related to the present Appeal which will directly affect, be directly affected by, or have a bearing on the Board's decision.

3.   Status of the Claims

Claims 3, 4, 6, 9, 10, 12, 22, and 23 are presently active.

Claims 3, 4, 9, 10, 22, and 23 stand rejected under 35 U.S.C. §102(b), as being anticipated by Kogan, US patent 5,321,656 ("Kogan"); and claims 6 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Figs. 1-4 in view of Kogan.

4. Status of Amendments

No amendment has been filed subsequent to the final rejection.

5. Summary of the Invention

The present invention is directed to a circuit for providing a local time-average minimum or a local time-average maximum of an input voltage signal. By a local time-average minimum, it is meant that the circuit provides an output voltage signal that follows a time-average of the input voltage signal. The circuit has a "finite memory" for averaging, so that if the input voltage signal were to decrease (increase) on average over a time interval greater than the finite memory of the circuit, then the output voltage signal would also decrease (increase) in time to reflect the new time-average minimum. Similar remarks apply when the circuit is configured to provide a local time-average maximum.

The "memory" of the circuit is set by the leakage current of a transistor. The claims recite that the transistor leakage current is in excess of 1 micro ampere per micron of device width.

Furthermore, the claims include the claim limitations of either an output voltage that is indicative of a local time-average maximum of the input voltage signal, or a local time-average minimum of the input voltage signal.

6. Issue

Whether claims 3, 4, 6, 9, 10, 12, 22, and 23 are patentable over Kogan.

7. Grouping of Claims

Applicants assert that all of the claims at issue fall into one group.

All of the claims recite the limitation that the leakage current is in excess of 1 micro ampere per micron of device width, and recite that the output voltage is either indicative of a local time-average maximum of the input signal voltage, or a local time-average minimum of the input signal voltage.

8.   Argument

In the most recent office action mailed 20 February 2004 ("Office Action"), Figs. 1C and 8C of Kogan were cited for teaching claims 3, 4, 9, 10, 22, and 23. But it is taught in Kogan that these circuits are used either to provide a maximum or a minimum of an input voltage signal, not a local time-average maximum or minimum.

Upon reading the specification describing Figs. 1A through 1D, it is to be understood that in Fig. 8C, nodes a and b are discharged to ground during a "pre-charge" interval by turning ON transistors Q2 and Q3. During an acquisition interval, nodes a and b are isolated from ground by turning OFF transistors Q2 and Q3, and node a is coupled to SIGNAL line by turning ON transistor Q1. The voltage at node b follows upward the voltage at node a, minus the threshold voltage value of transistor Q4. The voltage at node b will eventually provide the maximum of the voltage at node a (minus the threshold voltage value). However, the voltage at node b will not follow downward the voltage of node a if the voltage at node a were to decrease during the acquisition interval. This is so, because it is taught in Kogan, column 4, beginning at line 15, in regard to Figs. 1A and 2, that "when the SIGNAL and node a start to increase in voltage, node b cannot follow, but rather retains the lowest voltage that it was discharged to as it followed node a down." In understanding Fig. 8C from Fig. 1A, in the preceding quote from Kogan, "decrease" is to be substituted for "increase", "highest" for "lowest", "charged" for "discharged", and "up" for "down".

Therefore, as taught in Fig. 8C of Kogan, the voltage at node b cannot be the local time-average maximum of the input signal voltage. There is no time averaging involved. The circuit Fig. 8C of Kogan is a peak detector. Similarly, Kogan does not teach a voltage that provides the time-average minimum of the input signal voltage.

It is argued in the Office Action, at the top-half of page 5, that although Kogan does not disclose that the output voltage is indicative of a local time-average

maximum/minimum of the input signal, the output voltage is still inherently the local time-average maximum/minimum of the input signal. But there is no evidence that the output voltage is inherently a local time-average maximum or minimum. Indeed, Kogan teaches maximum or minimum detection, not local time-averaging. The circuit of Kogan would have the property claimed if there is sufficient leakage current, but then it wouldn't provide the maximum or minimum as taught by Kogan.

On page 3 of the Office Action, Dai, et al., US patent 6,339,347 ("Dai") is cited for teaching leakage current in excess of 1 micro ampere per micron of device width. As Applicant understands the Office Action, although two references are cited for a 35 U.S.C. §102(b) rejection, Dai is cited to argue that leakage current is inherent, and that therefore the claimed invention is inherent in Kogan. But again, as Applicant argued above, if such an amount of leakage current is inherent, then the device of Kogan would not provide a maximum or minimum, as taught by Kogan. Clearly, such an amount of leakage current is not necessarily present.

Indeed, usually leaky transistors are not desirable, and a considerable amount of research is devoted to either creating small devices that are not so leaky, or designing new circuit structures that mitigate the effects of such leakage. Dai teaches the use of an nMOS transistor having zero or negative threshold voltage in a particular circuit. As Dai states in column 4, starting at line 27, "the use of nMOS transistors having zero or negative threshold voltages in these traditional circuits results in wasteful power consumption due to the leakage current in the standby state." Usually, nMOS transistors having a positive threshold voltage are used because otherwise, as Dai teaches, there is wasteful power. However, for the particular circuit taught in Dai, this wasteful power is not a problem.

Therefore, Applicant believes it is incorrect to argue that the leaky transistors used in Dai are inherent in other circuits, such as that taught in Kogan.

Furthermore, all of the presently active claims include the claim limitation that the leakage current is in excess of 1 micro ampere per micron of device width. Clearly, this limitation is not taught by Kogan.

The above arguments apply to the other claim rejections, because only Kogan, along with Dai, are relied upon in the Office Action to teach the claimed transistor with

its gate tied to either its source or drain to provide the local time-average maximum or minimum, and as discussed above, Kogan does not teach a local time-average maximum or minimum, and the use of a leaky transistor as taught in Dai is not inherent in the circuit of Kogan.

Conclusion

For the above reasons, the Board is respectfully requested to vacate the Examiner's rejection of the pending claims, to remand this application to the Examiner, and to direct the Examiner to pass this case to issuance.

Respectfully submitted,

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9.   Appendix

1-2. (Cancelled)

3. (Previously Presented)   A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second

terminal;

wherein the gate and the first terminal are each connected to the input port, and

the second terminal is connected to the output port;

wherein the FET has a device width, wherein the FET has a leakage current in

excess of 1 micro ampere per micron of device width; and

wherein the output voltage is indicative of a local time-average maximum of the

input signal voltage.

4. (Previously Presented)   A method to provide an output voltage indicative of a local

time-average maximum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady

state and the input signal voltage is stationary, the FET having a gate, a first terminal, and

a second terminal, wherein the FET has a leakage current in excess of 1 micro ampere per

micron of device width, wherein the gate and the first terminal are each connected to an

input port, and the second terminal is connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port to provide a local time-average maximum of the input signal voltage.

5. (Cancelled)

6. (Previously Presented)   A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the gate and the first terminal are each connected to the input port, wherein the second terminal has a DC offset correction voltage, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width to provide the DC offset correction voltage as a local time-average maximum of the input signal voltage; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

7-8. (Cancelled)

9. (Previously Presented)   A circuit comprising:

an input port having an input signal voltage;

an output port having an output voltage; and

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal;

wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port;

wherein the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width; and

wherein the output voltage is a local time-average minimum of the input signal voltage.

10. (Previously Presented)   A method to provide an output voltage indicative of a local time-average minimum of an input signal voltage, the method comprising:

operating a field-effect transistor (FET) in its sub-threshold region when in steady state and the input signal voltage is stationary, the FET having a gate, a first terminal, and a second terminal, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width, wherein the first terminal is connected to an input port, and the gate and the second terminal are each connected to an output port;

providing the input signal voltage to the input port; and

sampling the output voltage at the output port to provide a local time-average minimum of the input signal voltage.

11. (Cancelled)

12. (Previously Presented)   A circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising:

an input port having the input signal voltage;

a field-effect-transistor (FET) having a gate, a first terminal, and a second terminal, wherein the first terminal is connected to the input port, wherein the gate and the second terminal are connected to each other and have a DC offset correction voltage; wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width to provide the DC offset correction voltage as a local time-average minimum of the input signal voltage; and

a DC offset correction unit responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage.

13-21. (Withdrawn)

22. (Currently Amended)   The circuit as set forth in claim 3, further comprising an output circuit connected to the output port to provide a capacitive load.

23. (Currently Amended)   The circuit as set forth in claim 9, further comprising an output circuit connected to the output port to provide a capacitive load.